

1052 — Computer Engineering (Full Time) Digital Logic Design (1052233110)

Part A — 1 mark(s) each

Unit 1

1. In AND gate the inputs A and B produce the output as

- a) $A+B$
- b) $A-B$
- c) $A.B$
- d) A/B

Answer: C

2. A Nibble is string of _____bits.

3. Binary addition of two 1's gives a

- a) sum=1 with carry of 1
- b) sum=0 with carry of 0
- c) sum=1 with carry of 0
- d) sum=0 with carry of 1

Answer: D

4. ASCII stands for

- a) American Standard Code for Idea Interchange
- b) American Standard Code for Information Intelligence
- c) American Standard Code for Information Intellectual
- d) American Standard Code for Information Interchange

Answer: D

5. Decimal equivalent of Hexadecimal number B.

- a) 12
- b) 10
- c) 13
- d) 11

Answer: D

6. The 2's complement of a binary number 1101 is

- a) 1010
- b) 0010
- c) 0011
- d) 1111

Answer: C

7. The weight of Hexadecimal number is

- c) 16

Answer: C

8. BCD code is a
- a) Binary Coded Decimal Code
 - b) Binary Coded Data Code
 - c) Binary Coded Difference Code
 - d) Binary Coded Design Code

Answer: A

9. What is the output of OR gate when both inputs are high
- a) none
 - b) invalid
 - c) low
 - d) high

Answer: D

10. Octal number contains _____ number of values.

11. Which gate is called as Universal Logic gate
- a) OR
 - b) AND
 - c) NAND
 - d) EX-OR

Answer: C

12. Decimal equivalent of ASCII value A

- a) 66
- b) 63
- c) 65
- d) 64

Answer: C

13. Decimal equivalent of BCD code 0100

14. NOT gate is also called as

- a) Exclusive Gate
- b) Converter Gate
- c) Universal Gate
- d) Inverter Gate

Answer: D

15. Binary Subtraction: $1-1=$

- a) Difference=0 with Borrow=0
- b) Difference=1 with Borrow=1
- c) Difference=1 with Borrow=0
- d) Difference=0 with Borrow=1

Answer: A

16. NOR gate is the complement of

- a) AND gate
- b) OR gate
- c) EX-OR gate
- d) NAND

Answer: B

17. The 1's complement of 1010 is

- a) 0010
- b) 0101
- c) 1111
- d) 0111

Answer: B

18. NOT gate contains

- a) Only one input
- b) 2 inputs
- c) 4 inputs
- d) 8 inputs

Answer: A

19. Binary number has a radix of _____.

- d) 16

20. Which of the following is NOT a Binary subtraction method

- a) ordinary method
- b) 3's complement method
- c) 2's complement method
- d) 1's complement method

Answer: B

Unit 2

1. The purpose of combinational circuits is:

- a) Memory storage
- b) Arithmetic and logical operations
- c) Counting
- d) Clock generation

Answer: B

2. Which law is: $A \cdot (B + C) = AB + AC$?

- a) Idempotent
- b) Associative
- c) Distributive

d) Demorgan's

Answer: C

3. A 3-variable K-map has how many cells?

c) 12

d) 16

4. Which one is **not** a combinational circuit?

a) Multiplexer

b) Decoder

c) Flip-Flop

d) Adder

Answer: C

5. A half adder has:

a) 1 input, 1 output

b) 2 inputs, 1 output

c) 2 inputs, 2 outputs

d) 3 inputs, 2 outputs

Answer: C

6. An 8-to-1 multiplexer needs _____ selector line.

7. The complement of 0 is:

b) A'

8. A half subtractor has:

a) 2 inputs, 1 output

b) 3 inputs, 3 outputs

c) 3 inputs, 2 outputs

d) 2 inputs, 2 outputs

Answer: D

9. The purpose of K-map is:

a) To count numbers

b) To simplify Boolean expressions

c) To perform addition

d) To store data

Answer: B

10. A 3-to-8 decoder has:

a) 3 inputs, 8 outputs

b) 8 inputs, 3 outputs

c) 3 inputs, 3 outputs

d) 8 inputs, 8 outputs

Answer: A

11. A 2-bit comparator has outputs:

- a) $A > B, A < B$
- b) $A > B, A < B, A = B$
- c) Only $A = B$
- d) Only $A > B$

Answer: B

12. Sum of full adder is given by:

- a) $A + B + C_{in}$
- b) $A \oplus B$
- c) $AB + C_{in}$
- d) $A \oplus B \oplus C_{in}$

Answer: D

13. A 2-to-1 multiplexer has:

- a) 2 inputs, 1 output, 1 select line
- b) 2 inputs, 2 outputs
- c) 1 input, 2 outputs
- d) 2 inputs, 2 select

Answer: A

14. $A + A = ?$

- d) A'

15. Dual of $A + 0 = A$ is

- a) $A \cdot 1 = A$
- b) $A \cdot 0 = A$
- c) $A + 1 = A$
- d) $A \cdot 0 = A$

Answer: A

16. A demultiplexer is the reverse of:

- a) Decoder
- b) Adder
- c) Comparator
- d) Multiplexer

Answer: D

17. $A + A' = ?$

- a) A
- b) 0
- c) 1
- d) A'

Answer: C

18. Universal gates are:

- a) AND, OR
- b) NAND, NOR
- c) XOR, XNOR
- d) Decoder, Encoder

Answer: B

19. A 1-bit comparator compares:

- a) Two 1-bit numbers
- b) Two 2-bit numbers
- c) Two 3-bit numbers
- d) Two 4-bit numbers

Answer: A

20. A 4-to-2 encoder has how many output lines?

- d) 16

Unit 3

1. What is the output condition of SR Flip Flop when the inputs $S=R=1$?

- a) No Change
- b) Set
- c) Reset
- d) Not Used

Answer: D

2. Which of the below is the Sequential Logic Circuit?

- a) Flip Flop
- b) Adder
- c) Subtractor
- d) Data Selector

Answer: A

3. Which output conditions NOT exist in Flip Flops?

- a) Set
- b) Reset
- c) Change
- d) Toggle

Answer: C

4. D Flip Flop is also called as _____.

- a) Set Reset Flip Flop
- b) Delay Flip Flop
- c) Toggle Flip Flop
- d) Divide by 2 Counter

Answer: B

5. Based on the specific point in the clock triggering of Flip Flop can be classified into _____ different types.

c) Nothing

6. Synchronous counter is also called as _____.

a) Serial Counter

b) Ripple Counter

c) Parallel Counter

d) Decade Counter

Answer: C

7. In how many modes Shift Register can operate?

8. In Sequential Logic circuit, whose output depends not only on the present inputs, but also depends on the previous outputs because of

a) Memory

b) Inverter

c) Synchronization

d) Clock Pulse

Answer: A

9. In Parallel to Serial Converter the read operation is in the form of?

a) Parallel

b) Both Serial and Parallel

c) None Serial or Parallel

d) Serial

Answer: D

10. Which Flip Flop is called as Universal Flip Flop?

a) JK Flip Flop

b) SR Flip Flop

c) T Flip Flop

d) D Flip Flop

Answer: A

11. In Serial to Parallel converter the write operation is in _____ form.

a) None Serial or Parallel

b) Both Serial and Parallel

c) Serial

d) Parallel

Answer: C

12. The variation of 0 to 1 is called _____.

a) Negative Edge

- b) Positive Edge
- c) High Level
- d) Low Level

Answer: B

13. A 4-bit Counter will count the value from 0000 to _____.

- a) 1111
- b) 1010
- c) 0111
- d) 1110

Answer: A

14. Flip Flop is a _____ logic element.

- a) Unistable
- b) Bistable
- c) Tristable
- d) Nullstable

Answer: B

15. The variation of 1 to 0 is called as _____.

- a) High Level
- b) Low Level
- c) Negative Edge
- d) Positive Edge

Answer: C

16. T Flip Flop is known as _____.

- a) Delay Flip Flop
- b) Data Flip Flop
- c) Divide by 2 Counter
- d) Universal Flip Flop

Answer: C

17. In Synchronous Counter, the system clock pulse is applied to _____.

- a) First Flip Flop only
- b) Last Flip Flop only
- c) Second Flip Flop only
- d) All Flip Flop directly

Answer: D

18. Register to store n-bit word containing _____ number of Flip Flops.

- b) $2n$
- c) $n-1$
- d) $n/2$

19. Each Flip Flop is triggered by the output of previous Flip Flop is called as _____.

- a) Parallel Counter
- b) Serial Counter
- c) Up Counter
- d) Down Counter

Answer: B

20. Asynchronous Counter is also called as _____.

- a) Shift Register
- b) SIPO Converter
- c) Parallel Counter
- d) Ripple Counter

Answer: D

Unit 4

1. If you want to interface a switch with a TTL logic circuit, which of the following precautions is most important?

- a) Voltage level compatibility
- b) Current amplification
- c) Use of optical fiber
- d) High frequency filtering

Answer: A

2. Which of the following is an integrating ADC?

- a) Flash ADC
- b) Successive approximation ADC
- c) Dual slope ADC
- d) Parallel comparator ADC

Answer: C

3. Why are relays often used in digital interfacing?

- a) To convert AC into DC
- b) To control high-power loads using low-power signals
- c) To increase clock frequency
- d) To provide memory storage

Answer: B

4. Which is a major difference between TTL and CMOS logic families?

- a) TTL uses higher resistance
- b) CMOS consumes less power than TTL
- c) CMOS has higher noise immunity than TTL
- d) CMOS is slower than TTL

Answer: B

5. Which of the following is not a part of digital interfacing devices?

- a) Motor
- b) Solenoid
- c) Transformer
- d) LED

Answer: C

6. The R-2R ladder DAC is preferred over the weighted resistor DAC because:

- a) It is slower
- b) It consumes more power
- c) It cannot be implemented practically
- d) It requires only two resistor values

Answer: D

7. CMOS circuits generally operate with a supply voltage of:

- a) 1V
- b) 3–15V
- c) 50V
- d) 230V

Answer: B

8. In a weighted resistor DAC, the output voltage is proportional to:

- a) Weight of resistor physically
- b) Capacitor charging
- c) Binary weighted currents
- d) Input clock pulses

Answer: C

9. Which of the following applications requires an ADC?

- a) Controlling a stepper motor from digital pulses
- b) Switching a relay
- c) Digital-to-analog music system
- d) Digital temperature measurement

Answer: D

10. The principle of the Successive Approximation ADC is based on:

- a) Counting pulses
- b) Binary search algorithm
- c) Repeated integration
- d) Resistive ladder

Answer: B

11. If the clock frequency of a successive approximation ADC is doubled, then:

- a) Resolution decreases
- b) Accuracy decreases
- c) Conversion time decreases
- d) Output range decreases

Answer: C

12. Which of the following is NOT a type of sensor?

- a) Compiler
- b) Temperature sensor
- c) Pressure sensor
- d) Light sensor

Answer: A

13. Which device converts an electrical signal into light in digital interfacing?

- a) LED
- b) Relay
- c) Motor
- d) Solenoid

Answer: A

14. A DAC converts:

- a) High frequency to low frequency
- b) AC to DC
- c) Analog to Digital
- d) Digital to Analog

Answer: D

15. In digital interfacing, the function of a solenoid is to:

- a) Generate electrical signals from motion
- b) Store binary information
- c) Convert light into electricity
- d) Provide linear mechanical motion when energized

Answer: D

16. The output of a sensor is usually:

- a) Either analog or digital
- b) Always digital
- c) Always analog
- d) Only binary

Answer: A

17. Why is a dual slope ADC often used in digital voltmeters?

- a) Low resolution

- b) High speed
- c) Noise rejection
- d) Low cost only

Answer: C

18. In digital interfacing, sensors are primarily used to:

- a) Convert physical quantities into electrical signals
- b) Store digital data
- c) Amplify digital signals
- d) Provide power to digital circuits

Answer: A

19. Which ADC provides the highest accuracy but is relatively slow?

- a) Flash ADC
- b) Successive Approximation ADC
- c) Dual Slope ADC
- d) Counter type ADC

Answer: C

20. The main disadvantage of a weighted resistor DAC is:

- a) High speed
- b) Simple design
- c) Requirement of wide resistor range
- d) High accuracy

Answer: C

Unit 5

1. Which device uses NAND flash memory internally?

- a) RAM module
- b) DVD
- c) SSD
- d) Magnetic tape

Answer: C

2. SD cards are primarily used in:

- a) Power supplies
- b) Network switches
- c) Smartphones and cameras
- d) Oscilloscopes

Answer: C

3. Which operation stores data into memory?

- a) Memory Write
- b) Memory Read
- c) Access Time

d) Word Length

Answer: A

4. Which of the following is NOT a programmable device?

a) PLA

b) FPGA

c) PAL

d) TTL gate IC

Answer: D

5. PLA (Programmable Logic Array) consists of two programmable stages, namely:

a) Decoder and multiplexer

b) OR plane and XOR plane

c) NAND plane and NOR plane

d) AND plane and OR plane

Answer: D

6. Access time in memory refers to:

a) Time to retrieve data

b) Time to write one bit

c) Total memory available

d) Number of address lines

Answer: A

7. Which RAM type is faster but more expensive?

a) DRAM

b) SRAM

c) Flash RAM

d) NVRAM

Answer: B

8. Which type of ROM can be erased using ultraviolet light?

a) PROM

b) EPROM

c) EEPROM

d) Flash ROM

Answer: B

9. One major advantage of PLDs over fixed logic devices is:

a) Lower cost always

b) Reduced power consumption

c) Smaller chip size

d) Flexibility and reprogrammability

Answer: D

10. ROM can be best described as:

- a) Volatile and programmable
- b) Non-volatile and read-only
- c) Volatile and read-only
- d)

Non-volatile and volatile both

Answer: B

11. In PLA architecture, the AND plane is used for:

- a) Address decoding only
- b) Summing outputs
- c) Multiplexing signals
- d) Generating product terms

Answer: D

12. Fixed logic devices are different from programmable logic devices because:

- a) They can be reprogrammed anytime
- b) They always use flash memory
- c) They cannot be altered once manufactured
- d) They are slower than PLDs

Answer: C

13. Which is an example of a fixed logic device?

- a) PROM
- b) PLA
- c) FPGA
- d) Standard IC gates

Answer: D

14. The main advantage of a solid-state hard disk (SSD) over HDD is:

- a) Higher power consumption
- b) Less cost per GB
- c) Faster access time and durability
- d) Mechanical movement of parts

Answer: C

15. A pen drive is based on which technology?

- a) Magnetic storage
- b) Optical storage
- c) Flash memory
- d) Dynamic RAM

Answer: C

16. Which memory hierarchy level is fastest?

- a) Hard disk
- b) Registers
- c) Cache memory
- d) Main memory

Answer: B

17. Flash ROM differs from NVRAM mainly because:

- a) Flash ROM is volatile, NVRAM is not
- b) Flash ROM is block erasable, NVRAM retains data using battery backup
- c) Both are identical
- d) Flash ROM is faster in writing than NVRAM

Answer: B

18. The number of bits in each memory location is called:

- a) Word length
- b) Access time
- c) Address line
- d) Capacity

Answer: A

19. Which operation retrieves data from memory?

- a) Memory Read
- b) Memory Write
- c) Memory Access Time
- d) Memory Capacity

Answer: A

20. If a memory has 16 address lines, its capacity is:

- a) 64 KB
- b) 16 bytes
- c) 64 bytes
- d) 32 bytes

Answer: A

Part B — 10 mark(s) each

Unit 1

1. Convert the given Decimal number 324 to its equivalent Binary, Octal and Hexadecimal number?

Answer:

1. Decimal → Binary

Divide 324 by 2 repeatedly:

$324 \div 2 = 162$ remainder 0

$162 \div 2 = 81$ remainder 0

$81 \div 2 = 40$ remainder 1

$$40 \div 2 = 20 \text{ remainder } 0$$

$$20 \div 2 = 10 \text{ remainder } 0$$

$$10 \div 2 = 5 \text{ remainder } 0$$

$$5 \div 2 = 2 \text{ remainder } 1$$

$$2 \div 2 = 1 \text{ remainder } 0$$

$$1 \div 2 = 0 \text{ remainder } 1$$

Reading remainders from bottom $\rightarrow$ top: 101000100

$$324_{10} = 101000100_2$$

2. Decimal $\rightarrow$ Octal

Divide 324 by 8:

$$324 \div 8 = 40 \text{ remainder } 4$$

$$40 \div 8 = 5 \text{ remainder } 0$$

$$5 \div 8 = 0 \text{ remainder } 5$$

Reading bottom $\rightarrow$ top: 504

$$324_{10} = 504_8$$

3. Decimal $\rightarrow$ Hexadecimal

Divide 324 by 16:

$$324 \div 16 = 20 \text{ remainder } 4$$

$$20 \div 16 = 1 \text{ remainder } 4$$

$$1 \div 16 = 0 \text{ remainder } 1$$

Reading bottom $\rightarrow$ top: 144

$$324_{10} = 144_{16}$$

2. Construct any four gates by using only NOR Gates?

Answer:

1. NOT Gate using NOR

Connect both inputs of a NOR gate together.

Output will be the inversion.

$$Y = A \text{ NOR } A = \bar{A}$$

2. OR Gate using NOR

First, invert both inputs using NOT (built from NOR).

Then NOR the results.

$$Y = (\bar{A} \text{ NOR } \bar{B}) = A + B$$

3. AND Gate using NOR

Use De Morgan's theorem:

$$A \cdot B = (\bar{A} + \bar{B})$$

Invert inputs using NOT (NOR gates), then NOR them together.

4. EX-OR Gate using NOR

$$\text{Expression: } A \oplus B = (A \text{ NOR } B) \text{ NOR } (\bar{A} \text{ NOR } \bar{B})$$

Requires multiple NOR gates (4 or more).

3. Explain ASCII code with example?

Answer:

ASCII Code

ASCII stands for American Standard Code for Information Interchange.

It is a 7-bit (or 8-bit extended) coding system used to represent characters, numbers, and symbols in digital systems.

Each character is assigned a unique binary value so that computers can process and exchange text data.

Example:

The letter 'A' has an ASCII value of 65 in decimal, which is 1000001 in binary (7-bit).

The digit '5' has an ASCII value of 53 in decimal, which is 00110101 in binary.

4. Draw the circuit diagram and truth table of AND, OR, NOT and EX-OR gates?

Answer:

1. AND Gate

Output is 1 only if both inputs are 1.

$$ABY = A \cdot B$$

0 0 0

0 1 0

1 0 0

1 1 1

2. OR Gate

Output is 1 if any input is 1.

$$ABY = A + B$$

0 0 0

0 1 1

1 0 1

1 1 1

3. NOT Gate

Output is the inversion of input.

$$AY = \bar{A}$$

0 1

1 0

4. EX-OR (XOR) Gate

Output is 1 if inputs are different.

$$ABY = A \oplus B$$

0 0 0

0 1 1

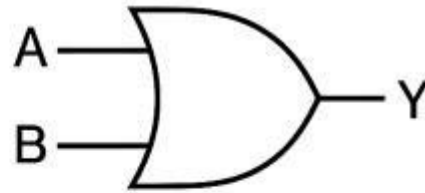
1 0 1

1 1 0

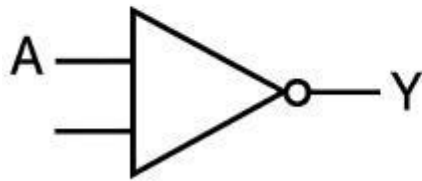
CIRCUIT DIAGRAM



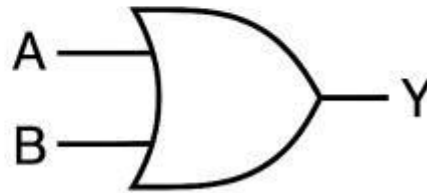
AND



OR



NOT



EX-OR

Unit 2

1. Prove DeMorgan's theorems with truth tables.

Answer: Prove DeMorgan's theorems with truth tables.

2. Explain the working of a 4-to-1 Multiplexer and a Priority Encoder with truth tables and applications?

Answer:

4-to-1 Multiplexer (MUX):

Definition: Selects one of 4 input (I_0, I_1, I_2, I_3) to send to the output, based on 2 selection lines (S_0, S_1)

Truth Table:

$S_1 S_0$ Output Y

00 I_0

01 I_1

10 I_2

11 I_3

Logic Expression: $Y = S_1' S_0' I_0 + S_1' S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3$

Applications: Used in data routing, function generation, and logic implementation.

Priority Encoder (4-to-2):

Definition: Converts multiple input lines into a binary code at the output, giving priority to the highest-order input.

Inputs: I_0, I_1, I_2, I_3

Outputs: Y_1, Y_0 (binary code), plus Valid Bit (V).

Truth Table:

I3I2I1I0Y1Y0V

1XXX111

01XX101

001X011

0001001

0000--0

Applications: Used in interrupt handling systems, digital systems requiring priority decisions.

3. Explain Half Adder with truth table and logic diagram.

Answer:

A Half Adder is a combinational circuit that performs the addition of two single-bit binary numbers. It has:

Inputs: A, B

Outputs:

Sum (S) → Result of addition

Carry (C) → Carry generated if both inputs are 1

Truth Table

AB Sum ($S = A \oplus B$) Carry ($C = A \cdot B$)

0 0 0	0
0 1 1	0
1 0 1	0
1 1 0	1

Logic Diagram

An XOR gate is used to generate the Sum.

An AND gate is used to generate the Carry.

A ---- $\oplus$ ---- > SUM (S)

XOR

B ---- $\oplus$

A ----- > CARRY (C)

AND

B -----

4. Compare pairs, quads and octets in K-Map with example?

Answer:

PAIRS: Two neighboring 1s in a K-map (horizontally or vertically adjacent) can be grouped.

Example: $A'B'CD + A'BC'D'$ reduced to $B'CD + BC'D'$

Each pair eliminates one variable from the Boolean expression. Here A is eliminated.

Reduces expression.

QUADS: A group of 4 adjacent 1s (can be square-shaped, row-wise, column-wise, or wrapping around edges).

Example: $A'B'CD + A'BC'D$ reduced to $B'C + BC'$

Each quad eliminates two variables. Here A'D is eliminated.

Further simplifies.

OCTETS: group of 8 adjacent 1s (covering half of the K-map).

Example: $A'B'C'D + A'BC'D$ reduced to $B' + B$

Each octet eliminates three variables. Here A'C'D is eliminated

Maximum simplification.

Unit 3

1. Explain the read and write operations in Parallel to Serial Converter?

Answer:

Parallel to Serial Converter

A Parallel-to-Serial Converter accepts data in parallel form (all bits at once) and then converts/transmits it one bit at a time serially with the help of a shift register.

1. Write Operation (Loading Parallel Data):

Apply the n-bit data word simultaneously at the parallel inputs of the register (D0, D1, D2, ... Dn).

Activate the LOAD (write) signal, which stores the parallel data into the flip-flops of the register.

After loading, each flip-flop holds its respective bit.

2. Read Operation (Shifting Out Serially):

Apply clock pulses to the shift register.

On each clock pulse, the stored data shifts one position to the right.

The bits come out serially from the last flip-flop (Qn), starting from the Most Significant Bit (MSB) or Least Significant Bit (LSB), depending on design.

After n clock pulses, the entire parallel word is transmitted in serial form.

3. Applications:

Used in serial communication systems (e.g., UART).

Efficient for data transmission over a single communication line.

Used in microprocessor systems for I/O conversions.

2. Demonstrate 4-bit Shift Register in detail?

Answer:

4-bit Shift Register

A shift register is a sequential circuit made of flip-flops, used to store and shift binary data.

A 4-bit shift register consists of four flip-flops connected in series, each capable of storing one bit.

1. Block Diagram:

Four D flip-flops (FF0, FF1, FF2, FF3) connected in cascade.

Common clock input applied to all flip-flops.

Data is shifted from one stage to the next with each clock pulse.

Serial Input → [FF0] → [FF1] → [FF2] → [FF3] → Serial Output (Q0) (Q1) (Q2) (Q3)

2. Working Principle:

On every clock pulse, the bit at the input shifts into the first flip-flop (FF0).

The previous bit in FF0 shifts to FF1, FF1 shifts to FF2, and FF2 shifts to FF3.

Thus, data moves one stage to the right with each clock pulse.

3. Types of 4-Bit Shift Registers:

Serial-In Serial-Out (SISO): Data enters serially and exits serially.

Serial-In Parallel-Out (SIPO): Data enters serially but can be read in parallel from Q0–Q3.

Parallel-In Serial-Out (PISO): Data loaded in parallel and shifted out serially.

Parallel-In Parallel-Out (PIPO): Data loaded and read out in parallel.

4. Truth Table (SIPO Example):

Clock Pulse Serial Input (D) Q0 Q1 Q2 Q3

1	1	1	0	0	0
2	0	0	1	0	0
3	1	1	0	1	0
4	1	1	1	0	1

5. Applications:

Data storage and transfer

Serial-to-parallel and parallel-to-serial conversion

Time delay circuits

Digital communication systems

3. Describe JK Flip Flop with Symbol, Logic Diagram and Truth table?

Answer:

JK Flip-Flop

A JK flip-flop is a universal flip-flop that eliminates the invalid state of the SR flip-flop. It has two inputs: J (Set) and K (Reset), along with Clock (CLK), output Q, and its complement $\bar{Q}$.

1. Symbol:

The symbol of JK flip-flop shows inputs J, K, CLK and outputs Q, $\bar{Q}$.

----|>----CLK | | J | | Q | | K | | $\bar{Q}$

2. Logic Diagram:

It is built using NAND gates (or NOR gates).

The J and K inputs are fed through gating logic controlled by the clock.

Feedback from the outputs ensures toggle action when $J=K=1$.

3. Truth Table:

J K CLK ($\uparrow$ edge) Q(next) Description

00 $\uparrow$	Q(prev)	No change (Hold)
01 $\uparrow$	0	Reset
10 $\uparrow$	1	Set
11 $\uparrow$	$\bar{Q}$	Toggle

Explanation:

When $J=1$, $K=0$, the flip-flop sets $Q=1$.

When $J=0$, $K=1$, the flip-flop resets $Q=0$.

When $J=K=0$, the output remains unchanged.

When $J=K=1$, the flip-flop toggles its state (Q changes from $0 \rightarrow 1$ or $1 \rightarrow 0$).

4. Elaborate Asynchronous Counter with Logic diagram and Waveform?

Answer:

Asynchronous Counter

An asynchronous counter (also called a ripple counter) is a type of counter where the flip-flops do not share the same clock signal. Instead, the output of one flip-flop acts as the clock input for the next flip-flop. Because of this, the outputs change at slightly different times, causing a ripple effect.

1. Working Principle:

The first flip-flop (LSB) is triggered by an external clock signal.

Each subsequent flip-flop is triggered by the output of the previous flip-flop.

This results in binary counting, but with a delay in propagation.

Example: A 3-bit asynchronous counter counts from 000 to 111 (0–7 in decimal).

2. Logic Diagram (3-bit Asynchronous Up Counter):

Clock $\rightarrow$ [T-FF0]–Q0 $\rightarrow$ [T-FF1]–Q1 $\rightarrow$ [T-FF2]–Q2

Each T flip-flop is configured to toggle ($T=1$).

$Q0 = \text{LSB}, Q2 = \text{MSB}.$

3. Truth Table (3-bit Counter):

Clock Pulses Q2 Q1 Q0 Decimal Count

0	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7

4. Waveform Explanation:

$Q0$ toggles on every clock pulse.

$Q1$ toggles when $Q0$ changes from 1 $\rightarrow$ 0.

$Q2$ toggles when $Q1$ changes from 1 $\rightarrow$ 0.

This produces a binary counting sequence with delays between outputs (ripple effect).

5. Drawbacks:

Slower due to propagation delay.

Not suitable for high-speed applications.

6. Applications:

Simple low-speed counters

Frequency division

Digital clocks and timers

Unit 4

1. Explain the working of Weighted Resistor DAC and R-2R Ladder DAC with circuit diagrams. Compare their advantages and disadvantages?

Answer:

Weighted Resistor DAC: binary-weighted resistors produce output current.

R-2R Ladder DAC: uses only R and 2R resistors for accuracy and scalability.

Draw circuit diagrams for both DACs.

Comparison: Weighted requires wide resistor range, R-2R simpler and accurate.

Mention applications in audio, control systems.

2. Explain different types of sensors used in digital systems with suitable examples and applications?

Answer:

Define sensors and their role in digital interfacing.

Types:

Temperature (LM35, thermistor),

Light (LDR, photodiode),

Pressure (piezoelectric),

Proximity (IR/Ultrasonic).

Explain analog vs digital sensors.

Applications in IoT, automation, robotics.

3. Compare TTL and CMOS logic families. Discuss their interfacing with switch, LED, relay, motor, and solenoid with neat diagrams?

Answer:

Define TTL (5V, higher power, faster) vs CMOS (3–15V, low power).

Explain voltage/current compatibility in interfacing.

Switch → logic input, LED → indicator, Relay → high power isolation, Motor/Solenoid → need driver circuits.

Provide block/circuit diagrams for at least LED and Relay interfacing.

4. Explain the working principle of Successive Approximation and Dual Slope A/D converters with neat diagrams. State their advantages and applications?

Answer:

Successive Approximation ADC: binary search method, uses SAR, fast conversion.

Dual Slope ADC: integrates input over time, rejects noise, used in digital voltmeters.

Compare speed, accuracy, and application areas.

Include block diagrams for both ADCs.

Unit 5

1. Differentiate between fixed logic and programmable logic devices (PLDs). Explain PLA architecture with a neat diagram?

Answer:

Fixed Logic Devices:

Perform only one specific function.

Cannot be reprogrammed after manufacturing.

Example: Standard logic gates, decoders, multiplexers.

Programmable Logic Devices (PLDs):

User-programmable for specific functions.

Examples: PAL, PLA, FPGA.

PLA Architecture:

Consists of a programmable AND array followed by a programmable OR array.

Inputs → AND array (to form product terms).

AND outputs → OR array (to form required sum of products).

Can implement complex combinational logic.

Diagram: Input lines → AND gates (programmable) → OR gates (programmable) → Output.

2. Differentiate between various types of ROM and RAM with suitable examples?

Answer:

Types of ROM:

Mask ROM: Data permanently stored during manufacturing.

PROM: Programmable once by the user.

EPROM: Erasable with UV light, reprogrammable.

EEPROM: Electrically erasable, byte-wise writable.

Flash ROM: High-speed reprogrammable memory used in USB drives and SSDs.

Types of RAM:

SRAM: Uses flip-flops, fast but costly, used in cache.

DRAM: Uses capacitors, cheaper, needs refreshing, used in main memory.

SDRAM/DDR: Synchronous with system clock, used in modern PCs.

Comparison Example: SRAM is 10 ns faster than DRAM but much more expensive, hence DRAM is widely used for main memory.

3. Explain memory hierarchy and management with the help of a neat diagram?

Answer:

Memory Hierarchy: Organizes memory into levels based on speed, cost, and size.

Registers: Fastest, smallest, inside CPU.

Cache: High-speed SRAM, stores frequently used data.

Main Memory (RAM): DRAM, larger but slower.

Secondary Storage: Hard disk/SSD, large, non-volatile, slower.

Tertiary Storage: Optical disks, magnetic tapes, archival storage.

Memory Management:

Ensures efficient use of available memory.

Includes allocation, protection, swapping, and virtual memory concepts.

Example: Operating systems use paging to map logical to physical addresses.

Diagram: (Registers → Cache → Main Memory → Secondary → Tertiary in pyramid form).

4. Explain in detail the different memory operations: memory read, memory write, access time, memory capacity, address lines, and word length with examples?

Answer:

Memory Read: Process of retrieving data from a specified memory location.

Memory Write: Process of storing data into a memory location.

Access Time: Time between a request and the data being available. Example: DRAM has higher access time than SRAM.

Memory Capacity: Total amount of data a memory can store, measured in bytes/GB.

Address Lines: Number of electrical lines used to select memory locations. If there are n address lines, memory can access 2^n locations.

Word Length: Number of bits the processor can process at a time, e.g., 8-bit, 16-bit, 32-bit processors.

These parameters together define how fast, efficient, and large the memory system is in a computer.

