

UNIT I – SWITCHING ALGEBRA AND LOGIC GATES

Part A

1. The binary equivalent of decimal 25 is:

- A) 11001 B) 10110 C) 10011 D) 11100

Answer: A

2. The radix of the hexadecimal number system

- A) 2 B) 8 C) 10 D) 16

Answer: D

3. 1's complement is obtained by:

- A) Adding 1 B) Reversing digits C) Changing 0 to 1 and 1 to 0 D) Multiplying by 2

Answer: C

4. 2's complement is obtained by:

- A) 1's complement + 1 B) Adding 2 C) Reversing bits D) Subtracting 1

Answer: A

5. Which gate is called the inverter?

- A) AND B) OR C) NOT D) XOR

Answer: C

6. Which gate produces HIGH only when all inputs are HIGH?

- A) OR B) NAND C) AND D) NOR

Answer: C

7. Boolean expression for an AND gate

- A) $A+B$ B) AB C) A' D) $A \oplus B$

Answer: B

8. Which is a universal gate?

- A) XOR B) AND C) NAND D) OR

Answer: C

9. Which gate is also a universal gate?

- A) NOR B) XOR C) AND D) NOT

Answer: A

10. De Morgan's first theorem

- A) $(AB)' = A' + B'$ B) $(A+B)' = A'B'$ C) Both A and B D) None

Answer: B

11. XOR gate output is HIGH when

- A) Inputs are same B) Inputs are different
C) All inputs HIGH D) All inputs LOW

Answer: B

12. XNOR gate is also called

- A) Equality gate B) NAND gate C) NOR gate D) Buffer

Answer: A

13. Positive logic represents logic 1 by

- A) Low voltage B) High voltage C) Zero voltage D) Negative voltage

Answer: B

14. Number of cells in a 4-variable K-map

- A) 4 B) 8 C) 16 D) 32

Answer: C

15. Boolean law $A+A$ equals

- A) 0 B) A C) 1 D) A'

Answer: B

16. $A \cdot 1$ equals

- A) 1 B) A C) 0 D) A'

Answer: B

17. $A+0$ equals

- A) 0 B) A C) 1 D) A'

Answer: B

18. Which gate gives LOW only when all inputs are HIGH?

- A) NAND B) NOR C) XOR D) OR

Answer: A

19. Binary of decimal 15 is

- A) 1010 B) 1111 C) 1100 D) 1001

Answer: B

20. Which gate performs logical addition?

- A) AND B) OR C) NOT D) NAND

Answer: B

21. Simplification of Boolean expressions is mainly done using

- A) Decoder B) K-map C) Encoder D) Comparator

Answer: B

22. Find the 2's complement of 101101

- A) 010011 B) 010010 C) 010001 D) 101101

Answer: A

23. Simplify $A+A'B$.

- A) $A+B$ B) AB C) A' D) B

Answer: A

24. Output of NAND gate for $A=1$, $B=1$.

- A) 0 B) 1 C) X D) Undefined

Answer: A

25. If $A=0$ and $B=1$, XOR output is

- A) 0 B) 1 C) 2 D) Undefined

Answer: B

26. Simplify $AB+AB'$

- A) A B) B C) $A+B$ D) 0

Answer: A

27. Simplify $(A+B)'$.

- A) $A'+B'$ B) $A'B'$ C) AB D) $A+B$

Answer: B

28. Decimal equivalent of binary 110101

- A) 53 B) 51 C) 54 D) 55

Answer: A

29. A logic function after K-map reduction gives fewer terms. The advantage is

- A) More power consumption B) More gates
C) Less hardware D) Higher delay

Answer: C

30. Which universal gate implementation requires the minimum number of gates for $F=(AB)'$?

- A) One NAND gate B) Two AND gates C) One OR gate D) Two NOT gates

Answer: A

Part B

1. Explain the different number systems (Binary, Octal, Decimal and Hexadecimal) and describe the methods of number system conversions with suitable examples.
2. State and prove De Morgan's theorems.
3. Explain the working, truth table and logic symbols of AND, OR, NOT, NAND, NOR, XOR and XNOR gates. Why are NAND and NOR called universal gates?
4. Explain Karnaugh Map (K-Map) minimization for 2-variable, 3-variable and 4-variable Boolean functions with suitable examples.
5. Simplify the Boolean function $F(A,B,C,D) = \sum m(0,2,5,7,8,10,13,15)$ using a 4-variable K-Map and implement the simplified function using logic gates only.

Unit II – Combinational Circuits

Part A

1. A combinational circuit is one in which the output depends on

- A) Present inputs only B) Previous outputs only
C) Clock pulse only D) Memory elements

Answer: A

2. The output of a Half Adder is

- A) Sum and Carry B) Difference and Borrow
C) Product and Carry D) Quotient and Remainder

Answer: A

3. The Sum output of a Half Adder is obtained using

- A) AND gate B) OR gate C) XOR gate D) NOR gate

Answer: C

4. The Carry output of a Half Adder is obtained using

- A) XOR gate B) AND gate C) OR gate D) NAND gate

Answer: B

5. A Full Adder has

- A) Two inputs B) Three inputs C) Four inputs D) One input

Answer: B

6. Which circuit can perform addition of three binary bits?

- A) Half Adder B) Full Adder C) Half Subtractor D) Comparator

Answer: B

7. The output of a Half Subtractor is

- A) Sum and Carry B) Difference and Borrow C) Difference and Carry D) Borrow only

Answer: B

8. A Full Subtractor has

- A) Two inputs B) Three inputs C) Four inputs D) One input

Answer: B

9. A comparator is used to

- A) Add numbers B) Compare binary numbers C) Store data D) Encode data

Answer: B

10. A 2×4 decoder has

- A) 2 inputs and 4 outputs
- B) 4 inputs and 2 outputs
- C) 2 inputs and 2 outputs
- D) 4 inputs and 4 outputs

Answer: A

11. A 4×2 encoder has

- A) 4 inputs and 2 outputs
- B) 2 inputs and 4 outputs
- C) 4 inputs and 4 outputs
- D) 2 inputs and 2 outputs

Answer: A

12. A Multiplexer is also called

- A) Data Selector
- B) Data Distributor
- C) Comparator
- D) Register

Answer: A

13. A Demultiplexer is also called

- A) Data Selector
- B) Data Distributor
- C) Encoder
- D) Decoder

Answer: B

14. A 4×1 Multiplexer has

- A) 4 inputs, 1 output
- B) 1 input, 4 outputs
- C) 2 inputs, 4 outputs
- D) 4 outputs only

Answer: A

15. The number of selection lines in a 4×1 MUX is

- A) 1
- B) 2
- C) 3
- D) 4

Answer: B

16. A parity generator is used to

- A) Store data
- B) Detect errors
- C) Amplify signals
- D) Compare numbers

Answer: B

17. Which parity makes the total number of 1's even?

- A) Odd parity
- B) Even parity
- C) Binary parity
- D) Gray parity

Answer: B

18. Tri-state logic has

- A) Two states
- B) Three output states
- C) Four output states
- D) One output state

Answer: B

19. The third state in tri-state logic is

- A) HIGH
- B) LOW
- C) High Impedance (Z)
- D) Ground

Answer: C

20. Which circuit selects one input from many inputs?

- A) Decoder
- B) Multiplexer
- C) Encoder
- D) Comparator

Answer: B

21. Which circuit activates one output corresponding to the binary input?

- A) Decoder
- B) Encoder
- C) MUX
- D) Comparator

Answer: A

22. A Half Adder receives $A = 1$ and $B = 1$. The outputs are

- A) Sum = 0, Carry = 1
- B) Sum = 1, Carry = 0
- C) Sum = 1, Carry = 1
- D) Sum = 0, Carry = 0

Answer: A

23. A Full Adder has inputs $A = 1$, $B = 1$, $C_{in} = 1$. The outputs are

- A) Sum = 1, Carry = 1
- B) Sum = 0, Carry = 1
- C) Sum = 1, Carry = 0
- D) Sum = 0, Carry = 0

A) NAND/NOR gates B) XOR gates C) AND gates only D) OR gates only

Answer: A

4. The invalid condition of an SR flip-flop occurs when

- A) S=0, R=0 B) S=1, R=0 C) S=0, R=1 D) S=1, R=1

Answer: D

5. Which flip-flop eliminates the invalid state of the SR flip-flop?

- A) D Flip-flop B) JK Flip-flop C) T Flip-flop D) RS Latch

Answer: B

6. The D flip-flop is also known as

- A) Delay flip-flop B) Toggle flip-flop C) Master flip-flop D) Reset flip-flop

Answer: A

7. A T flip-flop changes its state when

- A) T = 0 B) T = 1 C) S = 1 D) R = 1

Answer: B

8. The JK flip-flop toggles when

- A) J=0, K=0 B) J=1, K=0 C) J=0, K=1 D) J=1, K=1

Answer: D

9. The Master-Slave JK flip-flop is used to eliminate

- A) Race-around condition B) Noise C) Parity error D) Propagation delay

Answer: A

10. A flip-flop stores

- A) 1 bit B) 2 bits C) 4 bits D) 8 bits

Answer: A

11. A register is a group of

- A) Gates B) Flip-flops C) Multiplexers D) Encoders

Answer: B

12. SISO stands for

- A) Serial In Serial Out B) Serial In Parallel Out
C) Parallel In Serial Out D) Parallel In Parallel Out

Answer: A

13. SIPO stands for

- A) Serial In Parallel Out B) Parallel In Serial Out
C) Serial Out Parallel In D) Parallel Out Serial In

Answer: A

14. PISO stands for

- A) Parallel In Serial Out B) Parallel In Parallel Out
C) Serial In Serial Out D) Serial In Parallel Out

Answer: A

15. PIPO stands for

- A) Parallel In Parallel Out B) Parallel In Serial Out
C) Serial In Parallel Out D) Serial In Serial Out

Answer: A

16. Shift registers are mainly used for

- A) Data storage and transfer B) Voltage regulation
C) Signal amplification D) Frequency generation

Answer: A

17. Which flip-flop has only one input?

A) JK B) D C) SR D) RS

Answer: B

18. Which input combination causes a JK flip-flop to reset?

A) J=1, K=0 B) J=0, K=1 C) J=1, K=1 D) J=0, K=0

Answer: B

19. Which input combination sets a JK flip-flop?

A) J=1, K=0 B) J=0, K=1 C) J=1, K=1 D) J=0, K=0

Answer: A

20. A sequential circuit generally requires

A) Clock signal B) Antenna C) Oscilloscope D) Comparator

Answer: A

21. Which device is used for serial-to-parallel data conversion?

A) SIPO Register B) PISO Register C) Decoder D) Encoder

Answer: A

22. In an SR flip-flop, if S=1 and R=0, the next state is

A) Set (Q=1) B) Reset (Q=0) C) Toggle D) Invalid

Answer: A

23. A JK flip-flop has J=1 and K=1. If the present output is 0, the next output is

A) 0 B) 1 C) Invalid D) High Impedance

Answer: B

24. A T flip-flop has T=1 and the present output is 1. The next output is

A) 0 B) 1 C) Invalid D) Undefined

Answer: A

25. A D flip-flop receives D=1 at the active clock edge. The next output is

A) 0 B) 1 C) Toggle D) Previous state

Answer: B

26. Which register should be used to convert serial data into parallel data?

A) SISO B) SIPO C) PISO D) PIPO

Answer: B

27. Four bits are loaded simultaneously and taken out one by one. Which register is used?

A) PISO B) SIPO C) SISO D) PIPO

Answer: A

28. If a Master-Slave JK flip-flop is used, the main advantage is

A) Reduced power B) Elimination of race-around
C) Increased memory D) Faster clock generation

Answer: B

29. A 4-bit PIPO register can store:

A) 1 bit B) 2 bits C) 4 bits D) 8 bits

Answer: C

30. A SISO register containing 1011 shifts one bit to the right on each clock pulse. Its primary application is

A) Serial data transmission B) Code conversion
C) Memory expansion D) Voltage conversion

Answer: A

Part B

1. Explain the construction, truth table, characteristic equation and applications of SR and T Flip-Flops.
2. Explain the race-around condition in JK Flip.
3. Explain the operation of any one Shift Registers with neat block diagrams and applications.
4. Compare Latches and Flip-Flops. Explain their characteristics and applications.
5. Explain the construction, truth table, characteristic equation and applications of JK and D Flip-Flops.

Unit IV – Counters and Memories

Part A

1. A counter is a
A) Combinational circuit B) Sequential circuit
C) Linear circuit D) Analog circuit
Answer: B
2. Which counter operates without a common clock?
A) Synchronous counter B) Ripple counter C) Ring counter D) Decade counter
Answer: B
3. Another name for an asynchronous counter is
A) Ripple counter B) Ring counter C) Johnson counter D) Up counter
Answer: A
4. In a synchronous counter
A) Flip-flops have separate clocks B) All flip-flops receive the same clock
C) No clock is used D) Only one flip-flop is used
Answer: B
5. An up counter counts in
A) Descending order B) Ascending order C) Random order D) Gray code only
Answer: B
6. A down counter counts in
A) Ascending order B) Descending order
C) Random order D) Binary-coded decimal only
Answer: B
7. A decade counter counts
A) 0 to 7 B) 0 to 9 C) 0 to 15 D) 1 to 10
Answer: B
8. A ring counter is constructed using
A) Shift registers B) Multiplexers C) Decoders D) Comparators
Answer: A
9. A Johnson counter is also known as
A) Twisted Ring Counter B) Ripple Counter
C) Binary Counter D) Decade Counter
Answer: A
10. SRAM stands for
A) Static Random Access Memory B) Serial RAM C) Simple RAM
D) Synchronous RAM

Answer: A

11. DRAM stands for

- A) Dynamic Random Access Memory B) Digital RAM C) Dual RAM
D) Data RAM

Answer: A

12. SRAM stores data using

- A) Capacitors B) Flip-flops C) Diodes D) Resistors

Answer: B

13. DRAM stores data using

- A) Capacitors B) Flip-flops C) Registers D) Transistors only

Answer: A

14. Which memory requires periodic refreshing?

- A) SRAM B) DRAM C) ROM D) EEPROM

Answer: B

15. ROM stands for

- A) Read Only Memory B) Random Output Memory
C) Read Output Memory D) Register Only Memory

Answer: A

16. Which memory is non-volatile?

- A) SRAM B) DRAM C) ROM D) Cache

Answer: C

17. EPROM can be erased using

- A) Electrical signal B) Ultraviolet light C) Heat D) Magnetic field

Answer: B

18. EEPROM can be erased using

- A) Ultraviolet light B) Electrical signal C) Heat D) Infrared rays

Answer: B

19. Flash memory is a type of

- A) EEPROM B) SRAM C) DRAM D) Cache

Answer: A

20. Which memory has the fastest access time?

- A) SRAM B) DRAM C) ROM D) EPROM

Answer: A

21. Which counter is commonly used in digital clocks?

- A) Decade Counter B) Ring Counter C) Ripple Counter D) Johnson Counter

Answer: A

22. A 4-bit binary up counter starts at 0000. After five clock pulses, its output is

- A) 0101 B) 0100 C) 0110 D) 0011

Answer: A

23. A decade counter is currently at 1001 (9). After one clock pulse, the output becomes

- A) 1010 B) 0000 C) 0001 D) 1111

Answer: B

24. Which counter has less propagation delay?

- A) Ripple Counter B) Synchronous Counter C) Ring Counter D) Johnson Counter

Answer: B

25. Which memory should be selected for high-speed cache memory?

- A) DRAM B) SRAM C) ROM D) EPROM

Answer: B

26. Which memory is best suited for the main memory of a computer because of its low cost and high density?

- A) SRAM B) DRAM C) ROM D) EEPROM

Answer: B

27. A 4-bit ring counter uses four flip-flops. How many unique states does it have?

- A) 2 B) 4 C) 8 D) 16

Answer: B

28. A Johnson counter with four flip-flops has

- A) 4 states B) 8 states C) 16 states D) 2 states

Answer: B

29. A system requires memory that retains data even after power is turned OFF and can be electrically reprogrammed. Which memory is suitable?

- A) SRAM B) DRAM C) EEPROM D) Cache Memory

Answer: C

30. If minimum propagation delay and simultaneous triggering of all flip-flops are required, which counter should be used?

- A) Ripple Counter B) Synchronous Counter C) Ring Counter D) Johnson Counter

Answer: B

Part B

1. Explain the working of Asynchronous (Ripple) Counter with neat logic diagrams.
2. Explain Mod-10 (Decade) Counter with logic diagrams and timing waveforms.
3. Explain Johnson Counter with neat diagrams and state sequences.
4. Compare SRAM, DRAM based on structure, operation and applications.
5. Design a 4-bit synchronous binary up counter using JK Flip-Flops. Draw the logic diagram and explain the counting sequence from 0000 to 1111 with timing analysis.

Unit V – Programmable Logic Devices, VLSI and VHDL

Part A

1. PLA stands for

- A) Programmable Logic Array B) Parallel Logic Array
C) Programmable Linear Array D) Program Logic Architecture

Answer: A

2. PAL stands for

- A) Programmable Array Logic B) Parallel Array Logic
C) Programmed Array Latch D) Programmable Arithmetic Logic

Answer: A

3. FPGA stands for

- A) Field Programmable Gate Array B) Fixed Programmable Gate Array
C) Field Program Gate Architecture D) Fast Programmable Gate Array

Answer: A

4. Which device provides the highest flexibility after manufacturing?

- A) ROM B) PLA C) FPGA D) PAL

Answer: C

5. A PLA has

- A) Fixed AND and Fixed OR arrays
- B) Programmable AND and Programmable OR arrays
- C) Fixed AND and Programmable OR arrays
- D) Programmable AND and Fixed OR arrays

Answer: B

6. A PAL consists of

- A) Programmable AND array and Fixed OR array
- B) Fixed AND and Fixed OR arrays
- C) Fixed AND and Programmable OR array
- D) Programmable OR array only

Answer: A

7. VLSI stands for

- A) Very Large Scale Integration
- B) Variable Large Scale Integration
- C) Very Low Scale Integration
- D) Virtual Logic System Integration

Answer: A

8. SSI stands for

- A) Small Scale Integration
- B) Super Scale Integration
- C) Simple System Integration
- D) Standard Scale Integration

Answer: A

9. MSI stands for

- A) Medium Scale Integration
- B) Maximum Scale Integration
- C) Modular Scale Integration
- D) Main System Integration

Answer: A

10. LSI stands for

- A) Large Scale Integration
- B) Low Scale Integration
- C) Logic Scale Integration
- D) Linear Scale Integration

Answer: A

11. HDL stands for

- A) Hardware Description Language
- B) High Definition Language
- C) Hardware Design Logic
- D) High Data Language

Answer: A

12. VHDL stands for

- A) VHSIC Hardware Description Language
- B) Virtual Hardware Design Language
- C) Visual Hardware Description Logic
- D) Very High Data Language

Answer: A

13. VHDL is mainly used for

- A) Hardware modelling
- B) Word processing
- C) Database management
- D) Networking

Answer: A

14. Which section of a VHDL program defines the input and output ports?

- A) Entity
- B) Architecture
- C) Package
- D) Process

Answer: A

15. The behavior of a circuit in VHDL is described in

- A) Entity B) Architecture C) Library D) Package

Answer: B

16. Which VHDL modeling style describes the circuit using Boolean equations?

- A) Dataflow Modeling B) Behavioral Modeling
C) Structural Modeling D) Sequential Modeling

Answer: A

17. Structural modeling in VHDL is based on

- A) Interconnecting components B) Truth tables only
C) Arithmetic operations only D) Timing diagrams

Answer: A

18. Behavioral modeling describes

- A) Circuit operation using algorithms B) Physical layout
C) Gate dimensions D) PCB design

Answer: A

19. Which programmable device is commonly used for rapid prototyping?

- A) PAL B) PLA C) FPGA D) ROM

Answer: C

20. Which VLSI design level is closest to the physical implementation?

- A) Behavioral Level B) Register Transfer Level
C) Gate Level D) Layout Level

Answer: D

21. VHDL code is converted into hardware using

- A) Compiler/Synthesis Tool B) Text Editor C) Assembler D) Interpreter

22. A digital system requires both programmable AND and programmable OR arrays. Which device is most suitable?

- A) PAL B) PLA C) ROM D) Decoder

Answer: B

23. A design needs to be reprogrammed many times during testing. Which device should be selected?

- A) PAL B) FPGA C) ROM D) PROM

Answer: B

24. In a VHDL program, if the inputs and outputs are declared incorrectly in the Entity section, what is the likely result?

- A) Successful synthesis B) Compilation error
C) Faster execution D) Reduced hardware

Answer: B

25. Which VHDL modeling style is best when designing a circuit by connecting logic gates and components?

- A) Behavioral B) Structural C) Dataflow D) Sequential

Answer: B

26. A designer wants to describe the output of an AND gate using the statement $Y \leq A \text{ AND } B$. Which modeling style is used?

- A) Dataflow B) Structural C) Behavioral D) Gate Delay

Answer: A

27. Which VLSI integration level typically contains thousands of logic gates on a single chip?

- A) SSI B) MSI C) LSI D) VLSI

Answer: D

28. A company needs a programmable logic device with lower cost and faster operation than a PLA, even though it offers less flexibility. Which device is preferred?

- A) FPGA B) PAL C) ROM D) SRAM

Answer: B

29. Which stage of VLSI design converts HDL code into a gate-level implementation?

- A) Simulation B) Synthesis C) Fabrication D) Packaging

Answer: B

30. A VHDL design is simulated before fabrication mainly to

- A) Increase chip size B) Verify the correctness of the design
C) Reduce memory capacity D) Increase clock frequency

Answer: B

Part B

1. Explain the architecture, operation, advantages and applications of PLA, PAL

2. a) Explain the different levels of VLSI integration

b) Discuss the VLSI design flow.

3. Explain the structure of a VHDL program.

4. Describe the Entity and Architecture blocks with examples.

5. Write a VHDL program for a 4:1 Multiplexer using Dataflow modeling. Explain the code, simulate the output for different select inputs, and verify the truth table.